# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 09-082944

(43)Date of publication of application : 28.03.1997

(51)Int.Cl. H01L 29/78

(21)Application number : 07-238755

(22)Date of filing : 18.09.1995

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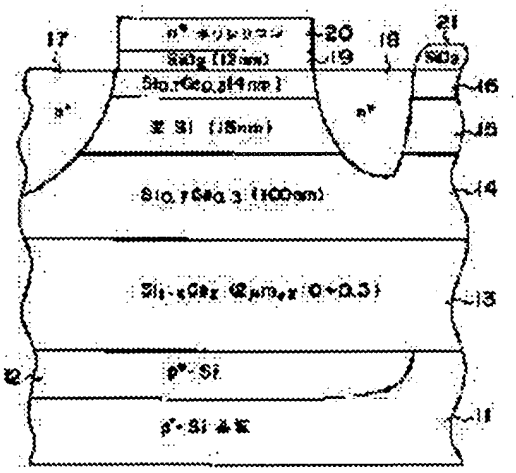
## (54) DISTORTION SILICON FIELD EFFECT TRANSISTOR AND MANUFACTURE OF THE SAME

(57)Abstract:

PROBLEM TO BE SOLVED: To improve the high electric field characteristic of buried type distortion silicon field effect transistor.

SOLUTION: SiGe buffer layers 13 and 14, a distortion silicon active layer 15 and an Si system compound semiconductor intermediate layer 16 are provided on a silicon substrate 11, and gate structures 19 and 20 are provided on the intermediate layer 16. The buffer layer 14 is connected to the silicon active layer with lattice relaxation and the intermediate layer 16 has a thickness smaller than the extension of an electron wave function.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or

application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to manufacture and its manufacture approach of a field-effect transistor.
[0002]
[Description of the Prior Art] Silicon has accomplished development from IC increasingly to LSI, VLSI, and ULSI for the reasons of the adaptability to the high dependability and planar technique etc. On the other hand, in light effective electron mass, a point with the comparatively easy band engineering by hetero structure, etc., a compound semiconductor has much charm compared with Si, judging from the electrical characteristics which the semiconductor material itself has. however, an advance of thin film crystal growth techniques, such as molecular beam epitaxy (MBE law) in recent years, a low voltage chemical-vapor-deposition method (LP-CVD method), and an ultra-high-vacuum chemical-vapor-deposition method (UHV-CVD method), -- a silicon system ingredient -- Si/Si1-x Gex etc. -- it becomes producible [ hetero structure ] and a high performance silicon system hetero device is being realized at an understanding and interval of silicon system hetero ingredient physical properties.
[0003] Si/Si1-x Gex Since it is accompanied by grid mismatching, the description of hetero epitaxial structure is to have connoted distortion. For this reason, the generated distorted thin films differ and the energy band structure in a heterojunction changes with the structures of a cascade screen according to it. A system interesting especially in physical properties is Si1-x Gex by which distortion was eased. It is the distorted silicon thin film which turned epitaxial growth up and was distorted by the tensile stress. It is known for this system that whenever [ electronic field internal transmigration ] will increase (for example, BORUGERUSANGU (Volgelsang) and Hoffmann (Hofmann), Applied Physics Letters, p.Vol.63 (1993) 186 reference). This is based on the following reasons.
[0004] That is, although the Fermi surface of bulk silicon is shown in drawing 7 (a), bulk silicon has six equivalent troughs in a conduction band, and only the number with an electron equal to each trough is distributed. Therefore, they are four troughs located in delta 2 and the remaining x-y flat surface in two troughs on the shaft (001) now shown by the drawing 7 (a) bullet delta 4 When expressed, with bulk silicon, it is delta 2. One third of total electron numbers is occupied. Moreover, each trough is not spherical and the effective mass changes with directions where nothing and an electron exercise the shape of a spheroid. For example, when the trough of a direction (001) is taken for an example, it is heavy, and is ml =0.92m0 (m0 is the electron mass in the inside of a vacuum), and the mass of a direction (001) is mass mt =0.19m0 [ light in a direction (inside of a x-y side) perpendicular to this ]. It has become. Now, compared with strain relaxation Si1-x Gex, it becomes low in energy in proportion to the presentation x of germanium. At distorted Si which turned epitaxial growth up, it is delta 2. delta 4 (refer to drawing 7 (b).) An energy level is divided and it is delta 2. delta 4 For example, it is reported by the People (IEEE Journal of QuantumElectronics, Vol.QE-22(1986) p.1696). . For this reason, delta 2 delta 4 Electronic [ most ] will be delta 2 if the value of x is enlarged enough at extent from which thermal excitation of a between does not become a problem (usually x> 0.2). It will be occupied.

[0005] Based on the above, the mobility when passing a current in a layer at parallel (inside of a x-y side) is considered. However, since it is easy, the quantum size effect which temperature is high enough and originates in a mass difference in this case is disregarded. Moreover, x values are fully large and all electrons are delta 2 at distorted Si. Suppose that it exists. Now, mobility is proportional to an effective mass. To there being contribution of both a heavy mass component and a light mass component with distortionlessness silicon, with distorted silicon, since it is only a light mass component, the effectual mass which is effective against mobility becomes light, and mobility increases. The growth factor of the mobility by this mass effect is (1/mt)/(4/6) (1/mt) (+ (2/6) (1-/ml))+3/(2+ (mt/ml)) =1.36. Furthermore, delta 2 of a trough delta 4 Energy separation causes control of valley dispersion. Especially, near the room temperature, many acoustic phonons exist, and since contribution of this valley dispersion is large, if the above-mentioned mobility growth factor becomes still larger to about 1.7, it is expected in above-mentioned BORUGERUSANGU's and others paper.

[0006] The structure and the energy band Fig. of a field-effect transistor which used distorted silicon for drawing 8 are shown (UERUZA et al. (Welser), IEEE Electron Device Letters, p.Vol.15 (1994) 100 reference). For the transistor shown in drawing 8 (a), the structure of an interface where induction of the two-dimensional electron is carried out is distorted Si/SiO2. It has become and distorted silicon MOS-FET is called. On the other hand, the transistor shown in drawing 8 (b) is distorted Si/Si0.7 germanium0.3 / SiO2. It has become, embedding mold distorted SiMOS-FET is called, and a two-dimensional electron is distorted Si and Si0.7germanium0.3. It has the intention of being accumulated in an interlayer's interface. In both of the structures, the SiGe buffer layer is growing first on Substrate Si. A SiGe buffer layer is the buffer layer with a concentration gradient of 1.5-micrometer thickness to which germanium presentation was gradually changed from 5% to 30%, and 0.25-micrometer Si0.7 germanium0.3 which was formed on it and by which grid relaxation was carried out. It is formed of the layer. The effectiveness of this buffer layer with a concentration gradient is Fitzgerald et al. (Fitzgerald) and Applied. Physics Si0.7 germanium0.3 by which is reported to Letters and Vol.59 (1991) 811 and grid relaxation was carried out Si0.7 germanium0.3 of original [ lattice constant / of a layer ] It eases completely to it of a layer, and a penetration rearrangement is stopped. Therefore, the lattice constant of Si layer which grew on the SiGe buffer layer is distorted. Moreover, since the thickness of this distorted Si layer is very as thin as about 10nm and it is smaller than critical thickness, a good crystal without a misfit rearrangement grows (critical thickness is indicated by the paper of the above-mentioned People, for example).

[0007] In addition, drawing 8 (a) and SiO2 shown in (b) of each The film is obtained by oxidizing thermally the epitaxial wafer which carried out crystal growth to distorted Si (gate oxidation). Therefore, the thickness of surface distorted Si is SiO2 which 10nm is consumed by gate oxidation and is 12nm although it was 16nm, growing in the structure of drawing 8 (a). The film is formed. Moreover, in the structure of drawing 8 (b), although the 10nm distorted Si layer of thickness had grown to be a front face, growing, all are consumed by gate oxidation. Generally, the oxide film of SiGe forms an interface trap level, and having a bad influence on properties, such as mobility of a component, is known, and it needs to consume a surface distorted Si cap layer completely by gate oxidation by embedding mold distorted SiMOS-FET of drawing 8 (b).

[0008] The property of the device by above-mentioned UEZURA and others was shown in drawing 9 as compared with usual silicon MOS-FET. Mobility is shown in the layer in the location where a two-dimensional electronic system exists as vertical effective electric field at drawing 9 (a). When effective electric field are small (<0.1 MV/cm), compared with the usual thing, as for mobility, a 2.9 times as many improvement as this is found by 1.8 times and embedding mold distorted silicon MOS-FET by distorted silicon MOS-FET. Thus, for the direction of embedding mold distorted silicon MOS-FET, this is Si/SiO2 although an improvement is found more. An interface is because electronic dispersion by the interface is large compared with a Si/SiGe hetero interface. However, it is high effective electric field and mobility will decrease sharply so that embedding mold distorted silicon MOS-FET may be looked at by drawing 9 (a). For this, at high electric field, an electron is SiO2 / Si0.7 germanium0.3. It is for beginning to collect on an interface. SiO2 / Si0.7 germanium0.3 An interface is Si/SiO2. It is coarser

than an interface and is Si0.7 germanium0.3 further. It is thought that mobility originates in it being smaller than the mobility of Si. Sharp decrease of the mobility in such high electric field of embedding mold distorted silicon MOS-FET has caused a rapid reduction of the mutual conductance in this component so that drawing 9 (b) may see.

[0009]

[Problem(s) to be Solved by the Invention] As explained above, conventional embedding mold distorted silicon MOS-FET is good Si/Si1-y Gey. Although it has big mobility compared with usual silicon MOS-FET in low electric field since the interface is used, in high electric field, a rapid reduction of mobility and reduction of the mutual conductance originating in this are caused, and the present condition is that the practical component is not obtained.

[0010] Moreover, in embedding mold distorted silicon MOS-FET, it is required to make equal thickness of the distorted silicon cap layer of the front face consumed by gate oxidation and thickness of the distorted silicon layer in epitaxial growth, and there was also a problem that the yield of a component became low, from the instability of an oxidation process or growth thickness control.

[0011] This invention was made in consideration of the above-mentioned situation, and the place made into the technical problem is in the thing which do not cause reduction in mobility by high electric field and for which it embeds and the mold distorted silicon electrolysis effectiveness transistor and its manufacture approach are offered.

[0012]

[Means for Solving the Problem] This invention has a grid relaxation buffer layer, a silicon barrier layer, and Si system compound semiconductor interlayer on a silicon substrate the 1st, it embeds, and in a mold distorted silicon field-effect transistor, said buffer layer touches said silicon barrier layer with grid relaxation, this barrier layer has internal distortion, and said interlayer provides this interlayer with the embedding mold distorted silicon field-effect transistor characterized by the thing for which gate structure was established, and which have thickness smaller than the breadth of an electron wave function.

[0013] A SiGe compound is usually used, a buffer layer has the presentation of Si1-x Gex (being here $0< x<=1$), and an interlayer may have the presentation of Si1-y Gey (here, it is $x<=y<=1$). Moreover, as for a buffer layer, it is desirable to have a concentration gradient about germanium. As other gestalten of a buffer layer, it is also possible to use the II-VI group compound semiconductor ZnSSe and the III-V group compound semiconductor InGaP.

[0014] This invention is the manufacture approach of the above-mentioned embedding mold distorted silicon field-effect transistor, and provides the 2nd with the approach characterized by making it grow up, without exposing a grid relaxation buffer layer, a silicon barrier layer, Si system compound semiconductor interlayer, and gate structure to atmospheric air on a silicon substrate.

[0015] Usually, epitaxial growth is followed in a grid relaxation buffer layer, a silicon barrier layer, and Si system compound semiconductor interlayer, and gate structure is continuously formed with the insulator layer formation equipment which also formed gate structure with the equipment which performed the epitaxial growth, or was connected with this epitaxial equipment by the high vacuum.

[0016] As for the embedding mold distorted silicon FET of this invention, the silicon system compound semiconductor interlayer (for example, Si1-y Gey) layer formed between a distorted silicon layer and gate structure is characterized by having thickness smaller than the breadth (about 5nm) of an electron wave function.

[0017] According to this invention, since the breadth of an electron wave function becomes smaller than an interlayer's thickness, also in high electric field, an electron's in interlayer existence probability can be sharply made small, it is controlled that the two-dimensional electron of Si / interlayer interface escapes to SiO2 / interlayer interface, and it becomes what has the few fall of mobility or a mutual conductance also in high electric field.

[0018] As for an interlayer's thickness, more specifically, it is desirable that they are especially 0.5nm thru/or 5nm. In addition, it may be based on the shot key barrier structure which formed conductive layers, such as a direct metal, as gate structure what [ not only ] is depended on an insulating layer /

conductive layer laminated structure but on the middle class.
[0019] Moreover, a gate oxidation process is unnecessary, and since each class is grown up without exposing to atmospheric air and there is no possibility that an interlayer may oxidize, it is possible according to the manufacture approach of this invention, to form SiO2 / interlayer interface of embedding mold distorted SiMOS-FET with a sufficient controllability for high quality.
[0020]
[The mode of implementation of invention] Hereafter, the mode of operation of this invention is explained. The outline sectional view of MOS-FET which starts drawing 1 at the mode of the 1st operation is shown. it is shown in drawing 1 -- as -- a surface field -- p+ p- in which the mold field 12 was formed the mold silicon substrate 11 top -- Si1-x Gex from -- the 1st becoming buffer layer 13 is formed in the thickness which is 2 micrometers. Si1-x Gex which constitutes this 1st buffer layer 13 It has the concentration gradient to which the presentation ratio x of germanium changed from the base continuously from zero to 0.3 towards the front face. On the 1st buffer layer 13, the 2nd buffer layer 14 is formed at the thickness which is 100nm. This 2nd buffer layer 14 consists of Si0.7 germanium0.3, and the lattice constant is eased on this buffer layer 14. On the 2nd buffer layer 14, it is formed at the thickness whose distorted silicon layer 15 is 15nm, and is Si1-y Gey with a thickness of 4nm on it. The laminating of the interlayer 16 is carried out. Si1-y Gey which constitutes an interlayer 16 Setting, the presentation ratio y of germanium is 0.3. Induction of the two-dimensional electron is carried out near the interface of an interlayer 16 and the distorted silicon layer 15. The source field 17 and the drain field 18 which reached the 2nd buffer layer 14 from the middle class 16, and were demarcated by the insulating layer 21 are formed. In addition, layers 13, 14, 15, and 16 are p molds, for example, are doped with the high impurity concentration of 1x1016cm-3. On an interlayer 16, they are silicon oxide 19 and n+. The laminating of the polish recon gate 20 is carried out, and it forms the embedding mold distorted silicon component.
[0021] Drawing 2 explains the effectiveness by this invention using the energy band Fig. and wave function of a conduction band edge. At drawing 2 (a), it is Si0.7 germanium0.3. The band Fig. corresponding to the mode of the 1st operation whose thickness d of the middle class 16 is 4nm is shown, and drawing 2 (b) shows the d= 9nm conventional example. The magnitude of effective electric field is both about 0.3 MV/cm. At the conventional example, wave function 51' is Si0.7 germanium0.3. It has the big amplitude by interlayer 16'. That is, the electron occupies in the SiGe interlayer and it has become the cause of a mobility fall. On the other hand, in this invention, as shown in drawing 2 (a), since the SiGe interlayer's 16 thickness is smaller than the breadth (about 5nm) of 4nm and a wave function, a wave function 51 does not have the amplitude in an interlayer 16, and degradation of mobility does not take place.
[0022] Drawing 3 plots mobility as a function of the effective electric field of the interface of layers 15 and 16 about the case where a SiGe interlayer's thickness d is 9nm, 6nm, and 4nm, in order to show the effectiveness of this invention. If an interlayer's thickness d becomes small with 9 to 6nm, mobility will become large in the same effective electric field. Under the same effective electric field, this is because the potential difference in an interlayer's both-ends side becomes small in proportion to thickness. However, a rapid reduction of mobility is looked at by both at the time of high effective electric field. This is because an electron is distributed over a SiGe interlayer as shown in drawing 2 (b). On the other hand, according to the effectiveness mentioned above, when an interlayer's thickness is set to 4nm, even if it becomes high effective electric field, most degradation of mobility is not seen.
[0023] MOS-FET shown in drawing 1 -- for example, a UHV-CVD method, LP-CVD method, and MBE -- it can manufacture with epitaxial growth continuously using law etc., without exposing to atmospheric air. If the example is given, first, in advance of growth, the ion implantation of the boron will be alternatively carried out to a substrate 11, and the p+-Si field 12 will be formed. After oxidizing a front face thermally after that, elevated-temperature heat treatment is performed, and the damage by ion implantation is recovered. In addition, the above process can be equivalent to well separation of c-MOS, and can be skipped depending on the case. After removing a surface oxide film by buffer fluoric acid, the 1st buffer layer 13 with a concentration gradient is grown up by equipping a UHV-CVD

system with a substrate, making a disilane and germane into material gas, and changing germane's quantity of gas flow gradually. Then, sequential growth of the 2nd buffer layer 14, distorted silicon layer 15, and interlayer 16 is carried out by controlling germane's flow rate. Diboron hexahydride can be used as material gas for p mold impurities of these layers. After growing up the SiGe middle class 16, a disilane and oxygen gas are introduced into coincidence, and it is SiO2. The film 19 is formed. In addition, SiO2 In film formation, it is a mono silane and H2 O2. The cotransduction of gas is also obtained. CVD on an oxide film usually becomes the polish recon instead of a crystal. Therefore, n+ The mold polish recon layer 20 can be easily formed within a UHV-CVD chamber, using an arsine as an impurity raw material. By the above growth flow, it is growing up by the growth chamber same from the SiGe buffer layer 13 to the polish recon layer 20. When there is no oxygen gas line in growth equipment, after forming an interlayer 16, a wafer is conveyed to other CVD systems etc. by high vacuum-ization of 1x10 to 4 or less Torrs, and it is SiO2. A layer 19 and the polish recon layer 20 can be formed. Conveyance under the high vacuum which is not exposed to atmospheric air can maintain the interface of an insulating layer 19 and an interlayer 16 at clarification.

[0024] The structure of drawing 1 is producible also by the conventional approach. In this case, the laminating of the silicon cap layer with a thickness of 10nm is carried out on the SiGe interlayer 16, it is thermal oxidation, and it is required to have consumed this silicon cap layer completely.

[0025] In addition, in the mode of implementation of the above 1st, it is Si1-y Gey. Although the middle class's germanium presentation y used the same value 0.3 as x of a SiGe buffer layer, y can take it (x<=y<=1). [ than x ] [ larger ]

[0026] (Mode of the 2nd operation) the voice of the 2nd operation to drawing 4 -- the outline sectional view of FET which starts like is shown. the voice shown in drawing 4 -- the voice which sets like and is shown in drawing 1 -- the voice shown on the SiGe buffer layer 31 at drawing 1 on the substrate 11 which can be set like, and the same substrate which is not illustrated -- the distorted silicon layer 15 which can be set like, and the same distorted silicon layer 32 are formed in the thickness which is 9nm. On this distorted silicon layer 32, it is Si1-y Gey. An interlayer 33 is formed and they are the thickness 15nmCaF insulating layer 36 and n+ on it. The polish recon layer 37 is formed. furthermore, the voice of drawing 1 -- the source field 17 and the drain field 18 which can be set like, the same source field 34 and the drain field 35, and the insulating layer 38 same in a list as an insulating layer 21 are also formed.

[0027] At the 1st embodiment, it is Si1-y Gey. Although an interlayer's 16 germanium presentation ratio y used the fixed value, it is possible to ease the electric field which the presentation ratio y is changed and are impressed to an interlayer 33. In order to make the electric field concerning an interlayer small effectually, as it is shown in drawing 5 (a), it is Si1-y Gey. The interface of an interlayer 33 and the distorted silicon layer 32 to Si1-y Gey What is necessary is just to make it the germanium presentation y increase toward the interface of an interlayer 33 and an insulator layer 36. Moreover, as shown in drawing 5 (b), the increment in this y may be gradual. Thus, when changing an interlayer's germanium presentation y, even if an interlayer's 33 thickness is larger than 5nm, there is no degradation of mobility to bigger electric field than the conventional example by the electric-field relaxation effect. However, if an interlayer's 33 thickness is set to 5nm or less and the electronic occupancy by the interlayer is controlled quantum-mechanically, there will be no degradation of mobility also at still higher electric field. This is the same as having explained drawing 2 and an essential target.

[0028] Moreover, in the 2nd mode, it is SiO2 as an insulator layer 36. Not the film but the CaF layer 36 is used. Other fluorides, such as BaSrF, can also be used instead of CaF. Fluoride insulator layers, such as CaF and BaSrF, can be formed by MBE. Furthermore, as a SiGe buffer layer 31, it is the buffer layer 13 with a concentration gradient and Si0.7 germanium0.3 which were shown in drawing 1 . Besides the combination of a buffer layer 14, you may be a superlattice buffer (for example, a chair miles (Ismail), Applied Physics Letters, Vol. 58 (1991) 2117 reference).

[0029] (Mode of the 3rd operation) the voice of the 3rd operation to drawing 6 -- the outline sectional view of FET which starts like is shown. This FET is the same as the structure shown in drawing 1 except having put the metal layer 41 rather than depending gate structure on silicon oxide 19 and the polish recon film 20, and having considered as shot key structure. Therefore, the same sign is given to the same

part as drawing 1 , and explanation is omitted.
[0030] In the mode of the above operation, it is Si1-y Gey as an interlayer. Although used and explained, it is Si1-y-z Gey Cz. You may be mixed crystal. Moreover, a distorted Si barrier layer may be a distorted SiGe barrier layer with germanium presentation smaller than the minimum value of germanium presentation of an interlayer. In addition, it can deform variously in the range which does not deviate from the summary of this invention.
[0031]
[Effect of the Invention] As explained above, according to this invention, the practical device using the Si/SiGe interface of high quality which embeds and does not have degradation of mobility or a mutual conductance in high effective electric field in mold distorted silicon FET can be obtained.

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[Translation done.]